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JUL 1 2 2004

Docket No. AMDP796US

H1930

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re **PATENT** application of:

Applicant: James Pan et al.

Application No.: 10/634,042

For: A DUAL-LEVEL STACKED FLASH MEMORY CELL WITH A MOSFET STORAGE TRANSISTOR

Filing Date: August 4, 2003

Examiner: Son Luu Mai

Art Unit: 2818

**REPLY TO OFFICE ACTION DATED JUNE 14, 2004**

Box Amendment  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

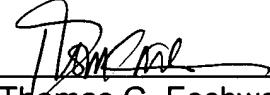
In response to the restriction requirement, applicant hereby elects Group II corresponding to claims 14-19 with traverse.

The election of Group II is made with traverse because the Examiner has failed in meeting his burden of showing that the inventions cited in Groups I, II, III, IV, and V are distinct. In addition, it is believed that a portion of the subject matter relating to the highlighted groups are common to the allegedly distinct inventions and thus searching the two groups would not constitute an undue burden. Furthermore, it is believed that prosecution of the claim groups may raise similar issues of patentability and thus compels a single examination of the claims.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP796US.

Respectfully submitted,  
ESCHWEILER & ASSOCIATES, LLC

  
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Thomas G. Eschweiler  
Registration No. 36,981

National City Bank Building  
629 Euclid Avenue, Suite 1210  
Cleveland, Ohio 44114  
(216) 502-0600

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Box Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: July 7, 2004

  
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Christine Gillroy